**Layout Rules and Guidelines**

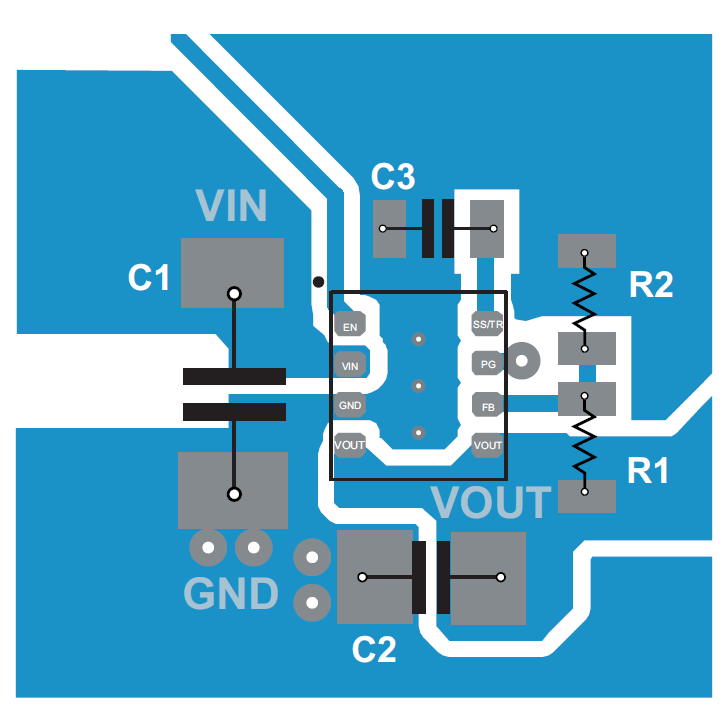
* **General**
  + Use 45 degree bends on all traces.
  + Locate discrete components close to their respective ICs as shown in the schematic diagram unless addressed specifically in this document.
* **Stackup**
  + Sample stackup shown in figure below; see stackup PDF for more information.



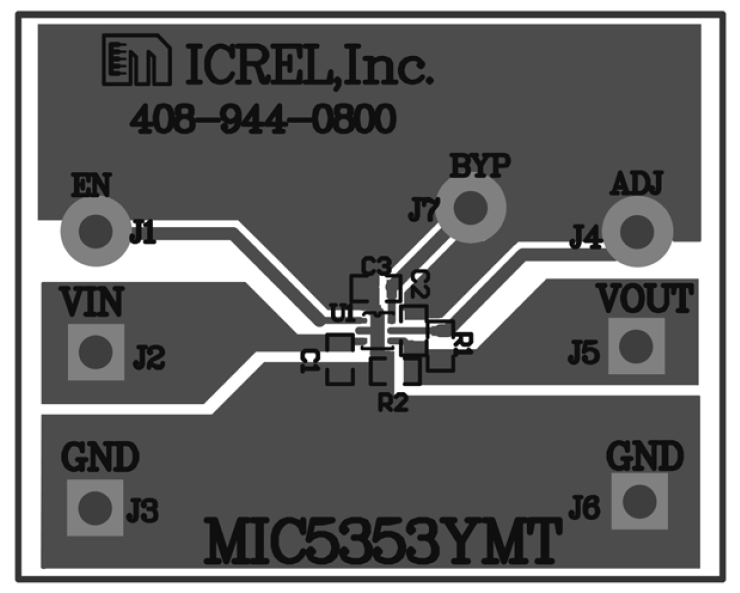
* + Thickness: **0.7874mm**
  + Material: **FR-4 or equivalent**
  + 4 layers
    - L1 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
    - L2 - GND
      * Thickness: 1oz
    - L3 - PWR
      * Thickness: 1oz
    - L4 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
* **Routing Rules**
  + Power (assumes 1oz copper, inner layers)
    - High Power: 2.03mm (80mil) minimum width
      * Signals: 5V0, GND
    - Medium Power: 0.83mm (32mil) minimum width
      * Signals: 12V0
    - Low Power: 0.3mm (12mil) minimum width
      * Signals: 3V3
    - All Others: 0.254mm (10mil) minimum width
      * Signals: VDDA
  + JTAG/Programming
    - Signals: MCU\_SWCLK, MCU\_SWDIO
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1 and 4
    - Maximum trace length of 100mm (4 inches).
    - Route signals so that there are no stubs.
    - Keep traces at least 3H away from other signals.
  + USB
    - Signals: MCU\_USB\_D\_P/N
    - Impedance: 90Ω ± 10% differential
    - Routing Layers: Layers 1 and 4
    - Trace lengths should be matched within 3.81mm (150mil) between pairs
    - Route signals so that there are no stubs.
    - A maximum of 1 via may be used along the full trace length.
    - Ground stitching vias should be placed within 1.27mm (50mil) of signal transitions from Layer 1 to Layer 4.
    - Traces should not be routed under or between pins of other devices
    - Traces and vias should be kept at least 3H away from other signals/fills.
  + Clocking
    - Signals: XI, XO, XO\_R
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1 and 4
    - Keep traces at least 3H away from other traces.
    - Route signals so that there are no stubs.
    - Ensure that crystal traces are matched within 0.127mm (5mil) of each other.
    - The maximum total trace length is 19mm (750mil).
  + General
    - Do not split signal ground planes.
    - Do not route signals over splits in reference planes.
    - Fill unused PCB areas with GND fills/planes.
    - Add ground-stitching vias every 6.35mm (250mil) in ground planes and fills; Stitch the edge of ground planes with vias.
    - Route traces on adjacent layers perpendicular to each other to reduce crosstalk.
    - Keep all clock lines as short as possible.
    - Do not route traces within 10H of a plane.
    - Do not share power and ground pads or use long, narrow traces for decoupling capacitors.
    - Make traces to power supply filtering components as short and wide as possible; vias should be used instead of long, narrow traces to connect to power planes.
    - Do not route traces under crystals and oscillators.
    - Use dogbones instead of via-in-pad.
  + Others
    - Keep noisy, high-frequency (i.e. high-speed digital and clock) signals away from Y1 and its capacitors.
* **Placement Guidelines**
  + Place D1-D4, J1, U1-U3 and Y1 as shown in figure below.



* Place C2-C6 near their associated pins on U1.
* Place L1 and C7-C8 near their associated pins on U1.
* Place C1 and R6-R8 near their associated pins on U1.
* Place R1 and Y1 near their associated pins on U1.
* Place C9-C11 and R9-R11 as close as possible to their associated pins on U2.
* Connect the exposed thermal pad of U2 to bottom or internal GND layer using vias.
* Use figure below for example layout of U2.



* Place C12-C14 as close as possible to their associated pins on U3.
* Use figure below for example layout of U3.



* + Place Y1 above a solid GND plane; connect a guard ring around Y1 if additional protection is needed.
* **Mechanical**
  + Please see the figure below of the MCO for dimensions and hole sizes:



* + Board Thickness: **0.7874mm**
  + Height restrictions (see figure below for more information)
    - Top Layer: **1.6mm**
    - Bottom Layer: **1.5mm**



* **Manufacturing**
  + No thermals should be used in this design.
  + Please add the fab number (**MOM-S-FAB-V1**) in copper on either the top or bottom layer in a corner of the board.
  + If the board house uses an internal tracking number and/or barcode, it should either be placed in silkscreen or as a sticker on the board.
  + Create a silkscreen rectangle and place a sticker within the rectangle containing the following items:
    - The assembly board number (**MOM-S-ASSY-V1.0**)
    - A board number in the format **N** where ‘N’ is the board number