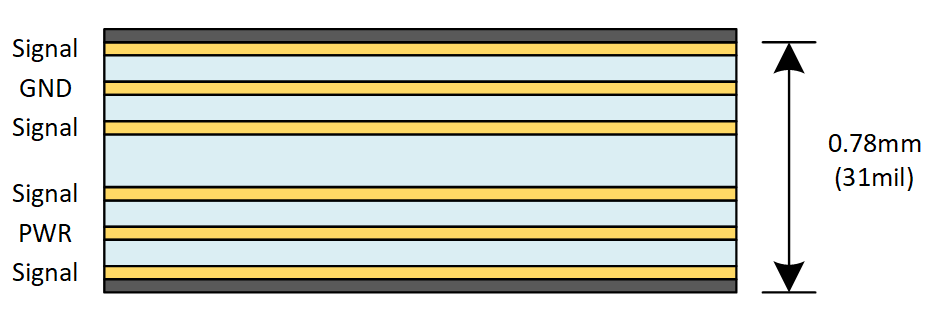
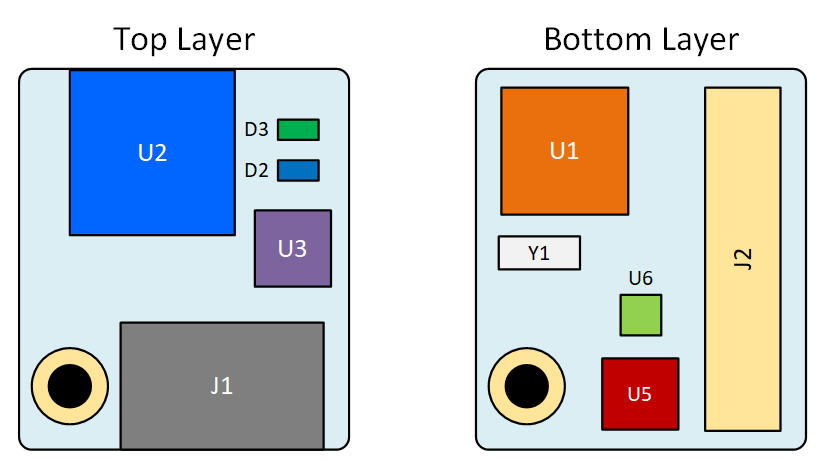
**Layout Rules and Guidelines**

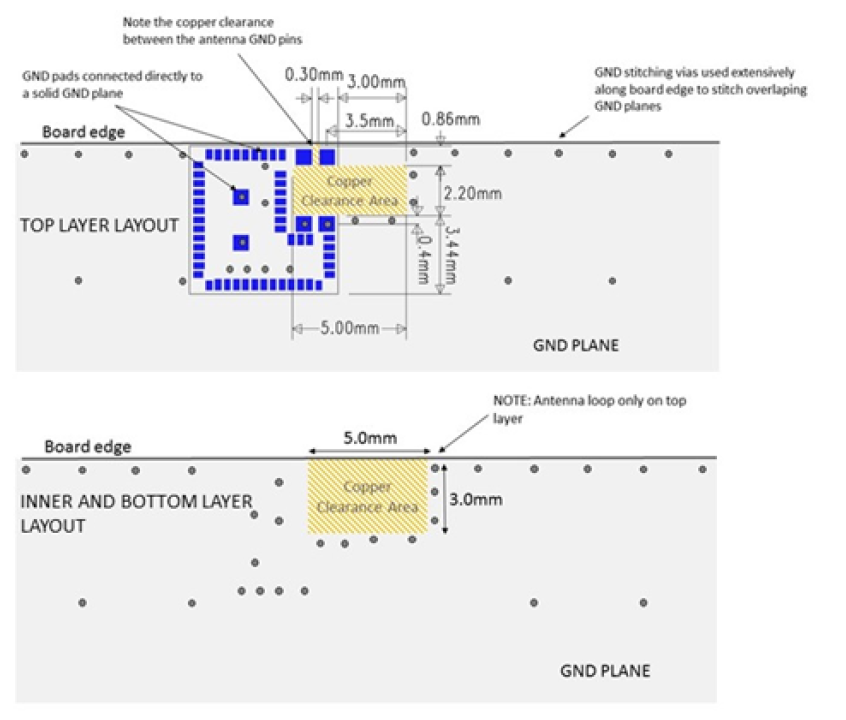
* **General**
  + Use 45 degree bends on all traces.
  + Locate discrete components close to their respective ICs as shown in the schematic diagram unless addressed specifically in this document.
* **Stackup**
  + Sample stackup shown in figure below; see stackup PDF for more information.



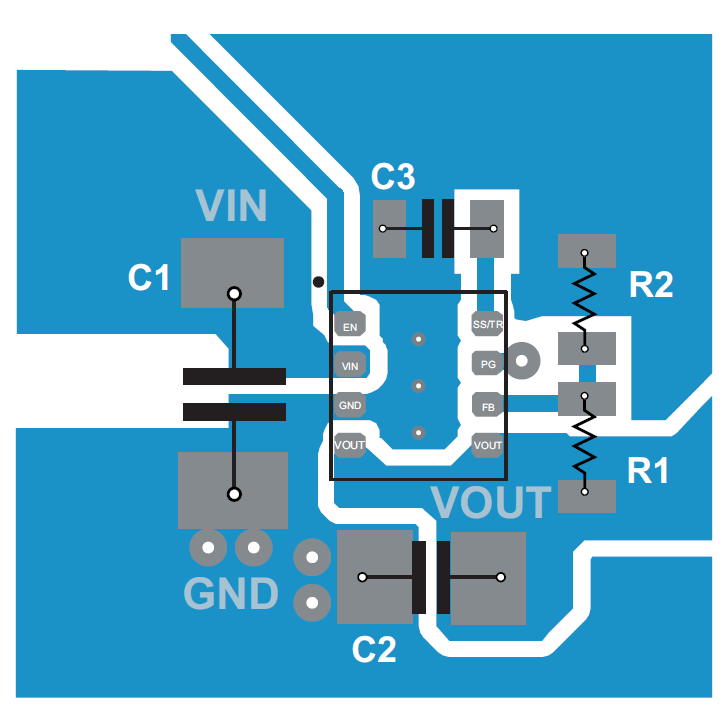
* + Thickness: **0.7874mm**
  + Material: **FR-4 or equivalent**
  + 6 layers
    - L1 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
    - L2 - GND
      * Thickness: 0.5oz
    - L3 - Signal
      * Thickness: 0.5oz
      * Impedances (±10%)
        + Single-ended: 50Ω
    - L4 - Signal
      * Thickness: 0.5oz
      * Impedances (±10%)
        + Single-ended: 50Ω
    - L5 - PWR
      * Thickness: 0.5oz
    - L6 - Signal
      * Thickness: 1oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
* **Routing Rules**
  + Power (assumes 0.5oz copper, inner layers)
    - High Power: 4.06mm (160mil) minimum width
      * Signals: 5V0, GND
    - Medium Power: 1.78mm (70mil) minimum width
      * Signals: 12V0
    - Low Power: 0.635mm (25mil) minimum width
      * Signals: 3V3, 5V0\_USB, VBUS
    - All Others: 0.254mm (10mil) minimum width
      * Signals: AVCC, VCCIO
  + JTAG/Programming
    - Signals: BT\_SWCLK, BT\_SWCLK, BT\_SWO, PDI\_CLK, PDI\_DATA
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1, 3, 4 and 6
    - Maximum trace length of 100mm (4 inches).
    - Route signals so that there are no stubs.
    - Keep traces at least 3H away from other signals.
  + USB
    - Signals: MCU\_D\_P/N, USB\_DR\_P/N, USB\_D\_P/N
    - Impedance: 90Ω ± 10% differential
    - Routing Layers: Layers 1 and 6
    - Trace lengths should be matched within 3.81mm (150mil) between pairs
    - Route signals so that there are no stubs.
    - A maximum of 1 via may be used along the full trace length.
    - Ground stitching vias should be placed within 1.27mm (50mil) of signal transitions from Layer 1 to Layer 6.
    - Traces should not be routed under or between pins of other devices
    - Traces and vias should be kept at least 3H away from other signals/fills.
    - Traces and vias should be kept at least 20H away from edge of the return plane.
  + Clocking
    - Signals: HFXO, XTALI, XTALO
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1 and 6
    - Keep traces at least 3H away from other traces.
    - Route signals so that there are no stubs.
    - Ensure that crystal traces are matched within 0.127mm (5mil) of each other.
    - The maximum total trace length is 19mm (750mil).
  + General
    - Do not split signal ground planes.
    - Do not route signals over splits in reference planes.
    - Fill unused PCB areas with GND fills/planes.
    - Add ground-stitching vias every 6.35mm (250mil) in ground planes and fills; Stitch the edge of ground planes with vias.
    - Route traces on adjacent layers perpendicular to each other to reduce crosstalk.
    - Keep all clock lines as short as possible.
    - Do not route traces within 10H of a plane.
    - Do not share power and ground pads or use long, narrow traces for decoupling capacitors.
    - Make traces to power supply filtering components as short and wide as possible; vias should be used instead of long, narrow traces to connect to power planes.
    - Do not route traces under crystals and oscillators.
    - Use dogbones instead of via-in-pad.
  + Others
    - Keep noisy, high-frequency (i.e. high-speed digital and clock) signals away from Y1 and its capacitors.
* **Placement Guidelines**
  + In general, ESD diodes should be placed closest to their associated connector, before any other components on the same signal (i.e. capacitors, inductors, etc).
  + Place D2-D3, J1-J2, U1-U3, U5-U6 and Y1 as shown in figure below.



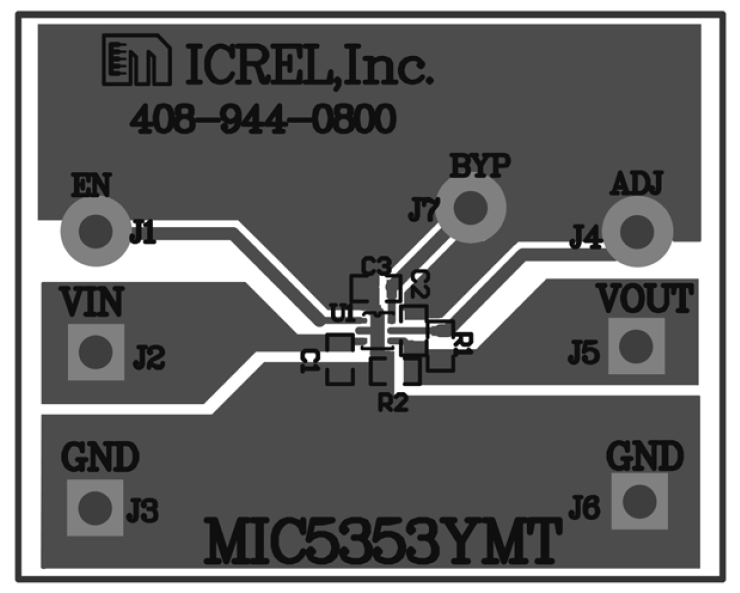
* Place C1-C4 near their associated pins on U1.
* Place L1 and C5-C6 near their associated pins on U1.
* Place R1 near its associated pin on U1.
* Place U2 at the edge of the PCB, as shown in the figure below; Do not place any metal (traces, components, battery, etc.) within the clearance area of the antenna shown in the figure below.



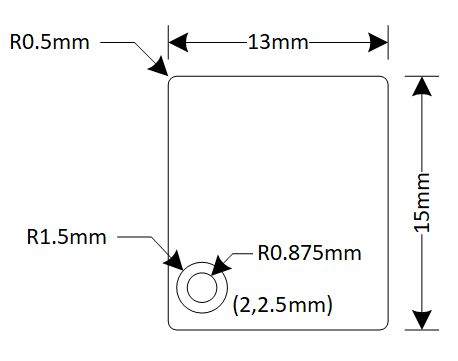
* Connect all ground pads of U2 directly to a solid ground plane.
* Place the ground vias for U2 as close to the ground pads as possible.
* A separation of at least 10mm is recommended between U2 and other metal materials; plastic has no effect on the antenna of U2.
* Place C7-C9 near their associated pins on U2.
* Place C12-C13 and C16 near their associated pins on U3.
* Place C14-C15, R3-R4 and R6-R7 near their associated pins on U3.
* Place C10, L2 and U4 near J1.
* Place C17-C18, C22 and R10-R12 as close as possible to their associated pins on U5.
* Connect the exposed thermal pad of U5 to bottom or internal GND layer using vias.
* Use figure below for example layout of U5.



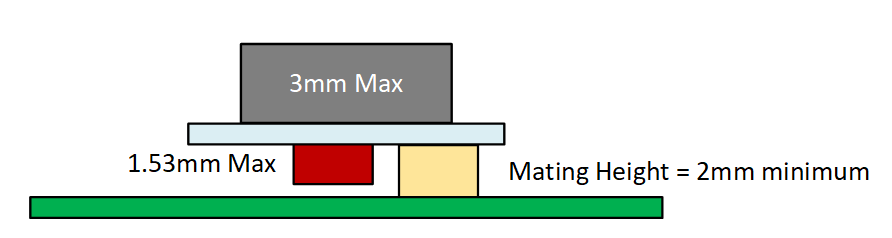
* Place C19-C21 as close as possible to their associated pins on U6.
* Use figure below for example layout of U6.



* + Place Y1 above a solid GND plane; connect a guard ring around Y1 if additional protection is needed.
* **Mechanical**
  + Please see the figure below of the MCO for dimensions and hole sizes:



* + Board Thickness: **0.7874mm**
  + Height restrictions (see figure below for more information)
    - Top Layer: **3mm**
    - Bottom Layer: **2mm**



* **Manufacturing**
  + No thermals should be used in this design.
  + Please add the fab number (**AMINO-FAB-V1**) in copper on either the top or bottom layer in a corner of the board.
  + If the board house uses an internal tracking number and/or barcode, it should either be placed in silkscreen or as a sticker on the board.
  + Create a silkscreen rectangle and place a sticker within the rectangle containing the following items:
    - The assembly board number (**AMINO-ASSY-V1.0**)
    - A board number in the format **N** where ‘N’ is the board number