**Layout Rules and Guidelines**

* **General**
  + Use 45 degree bends on all traces.
  + Locate discrete components close to their respective ICs as shown in the schematic diagram unless addressed specifically in this document.
* **Stackup**
  + Thickness: **0.7874mm**
  + Material: **FR-4 or equivalent**
  + 6 layers
    - L1 - Signal
      * Thickness: 0.5oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
    - L2 - GND
      * Thickness: 1oz
    - L3 - Signal
      * Thickness: 0.5oz
      * Impedances (±10%)
        + Single-ended: 50Ω
    - L4 - Signal
      * Thickness: 0.5oz
      * Impedances (±10%)
        + Single-ended: 50Ω
    - L5 - PWR
      * Thickness: 1oz
    - L6 - Signal
      * Thickness: 0.5oz + Plating
      * Impedances (±10%)
        + Single-ended: 50Ω
        + Differential: 90Ω
* **Routing Rules**
  + Power (assumes 1oz copper)
    - High Power: 50mil minimum width
      * Signals: <>
    - Medium Power: 20mil minimum width
      * Signals: <>
    - All Others: 10mil minimum width
      * <>
  + JTAG/Programming
    - Signals: BT\_SWCLK, BT\_SWCLK, BT\_SWO, PDI\_CLK, PDI\_DATA
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1, 3, 4 and 6
    - Maximum trace length of 4 inches.
    - Route signals so that there are no stubs.
    - Keep traces at least 3H away from other signals.
  + USB
    - Signals: MCU\_D\_P/N, USB\_DR\_P/N, USB\_D\_P/N
    - Impedance: 90Ω ± 10% differential
    - Routing Layers: Layers 1 and 6
    - Trace lengths should be matched within 150mil between pairs
    - Route signals so that there are no stubs.
    - A maximum of 1 via may be used along the full trace length.
    - Ground stitching vias should be placed within 50mil of signal transitions from Layer 1 to Layer 6.
    - Traces should not be routed under or between pins of other devices
    - Traces and vias should be kept at least 3H away from other signals/fills.
    - Traces and vias should be kept at least 20H away from edge of the return plane.
  + Clocking
    - Signals: HFXO, XTALI, XTALO
    - Impedance: 50Ω ± 10% single-ended
    - Routing Layers: Layers 1 and 6
    - Keep traces at least 3H away from other traces.
    - Route signals so that there are no stubs.
    - Ensure that crystal traces are matched within 5mil of each other.
    - The maximum total trace length is 750mil.
  + General
    - Do not split signal ground planes.
    - Do not route signals over splits in reference planes.
    - Fill unused PCB areas with GND fills/planes.
    - Add ground-stitching vias every 250mil in ground planes and fills; Stitch the edge of ground planes with vias.
    - Route traces on adjacent layers perpendicular to each other to reduce crosstalk.
    - Keep all clock lines as short as possible.
    - Do not route traces within 10H of a plane.
    - Do not share power and ground pads or use long, narrow traces for decoupling capacitors.
    - Make traces to power supply filtering components as short and wide as possible; vias should be used instead of long, narrow traces to connect to power planes.
    - Do not route traces under crystals and oscillators.
    - Use dogbones instead of via-in-pad.
  + Others
    - Keep noisy, high-frequency (i.e. high-speed digital and clock) signals away from Y1 and their capacitors.
* **Placement Guidelines**
  + In general, ESD diodes should be placed closest to their associated connector, before any other components on the same signal (i.e. capacitors, inductors, etc).
  + <>
* **Mechanical**
  + Please see the provided PcbDoc of the MCO for dimensions and hole sizes. A copy of this file has been reproduced in <> below.
  + Board Thickness: **0.7874mm**
  + Height restrictions
    - Top Layer: **3mm**
    - Bottom Layer: **2mm**
* **Manufacturing**
  + No thermals should be used in this design.
  + Please add the fab number (**XXXX-XXXXX**) in copper on either the top or bottom layer in a corner of the board.
  + If the board house uses an internal tracking number and/or barcode, it should either be placed in silkscreen or as a sticker on the board.
  + Create a silkscreen rectangle and place a sticker within the rectangle containing the following items:
    - The assembly board number (**XXXX-XXXXX**)
    - A board number in the format **XXXXX-N** where ‘N’ is the board number